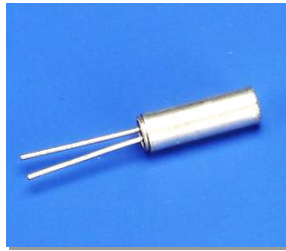


Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V

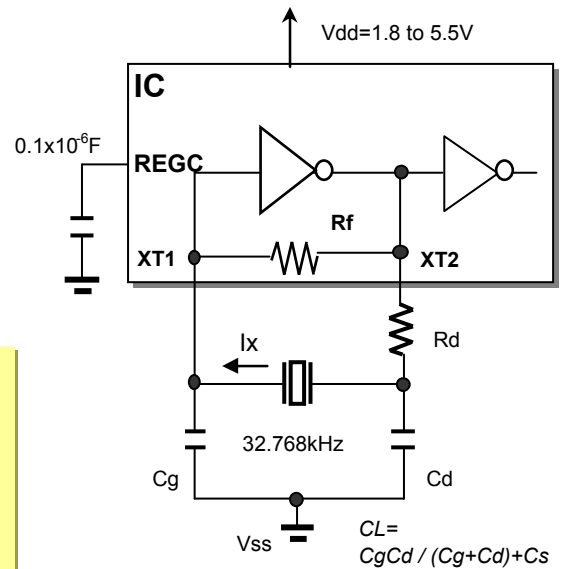
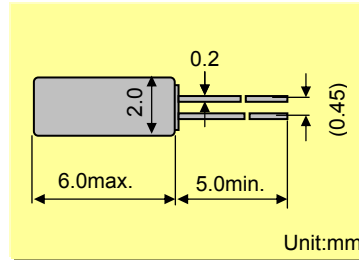


| | |
|------------------------------|--------------------------------|
| Model | :VT-200 |
| Frequency | :Fo=32.768kHz |
| Frequency tolerance | :dF/Fo= +/-20x10 ⁻⁶ |
| Load capacitance | :CL=12.5pF |
| Equivalent series resistance | :R1=50kohm max |
| Max. drive level | :DL=1x10 ⁻⁶ W max |
| Level of drivel | :DL=0.1x10 ⁻⁶ W typ |

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)

Remark) I_x : current through crystal

MODEL:VT-200 12.5pF with uPD78F1168GC at 25°C

| Key specifications | Low(*1) | Normal(*2) | Remarks |
|--|---------|------------|--|
| Current control resistance : R_d (k ohm) | 0 | 0 | Control drive level & secure phase margin |
| Capacitance at gate : C_g (pF) | (18) | (18) | Optimal capacitance in response to CL |
| Capacitance at drain : C_d (pF) | (18) | (18) | ($CL = C_d // C_g + \text{stray capacitance}$) |

| Circuit characteristics (at 25°C) | Low(*1) | Normal(*2) | Remarks |
|---|---------|------------|---|
| Matching Accuracy : df / f ($\times 10^{-6}$) | 2.1 | 4.9 | Frequency offset volume at specified V_{dd} |
| Voltage Fluctuation : $\pm df / V$ ($\times 10^{-6}$) | 0.0 | 0.0 | V_{dd} +/-10% (Standard operating voltage range) |
| Drive Level : DL ($\times 10^{-6}W$) | 0.13 | 0.22 | $DL = I_x^2 R_e < 1 \times 10^{-6}W, R_e = R_1(1 + C_o / CL)^2$ |
| Negative resistance : $ -RL $ (kohm) | 183 | 303 | 5 times larger than R_{1MAX} |
| Oscillation allowance : M (times) | 3.7 | 6.1 | Judgemental standard of oscillation stability |
| Voltage of oscillation start : V_{start} (V) | 1.60 | 1.60 | |
| Voltage of oscillation stop : V_{stop} (V) | 1.59 | 1.59 | |
| Oscillation start up time : T_s (sec) | 1.19 | 1.19 | Time to reach 90% of output level |

| Temperature characteristics of circuit | | Low(*1) | Normal(*2) | Remarks |
|--|---|---------|------------|--|
| at -40°C | Variation : df / T ($\times 10^{-6}$) | -145 | -145 | Typ.Tp=25°C ($K = -3.5 \times 10^{-8} / ^\circ C^2$) |
| at +85°C | Variation : df / T ($\times 10^{-6}$) | -126 | -126 | Typ.Tp=25°C ($K = -3.5 \times 10^{-8} / ^\circ C^2$) |

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

*1; low consumption current mode

*2; normal current mode

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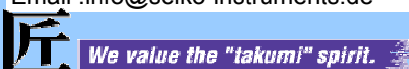
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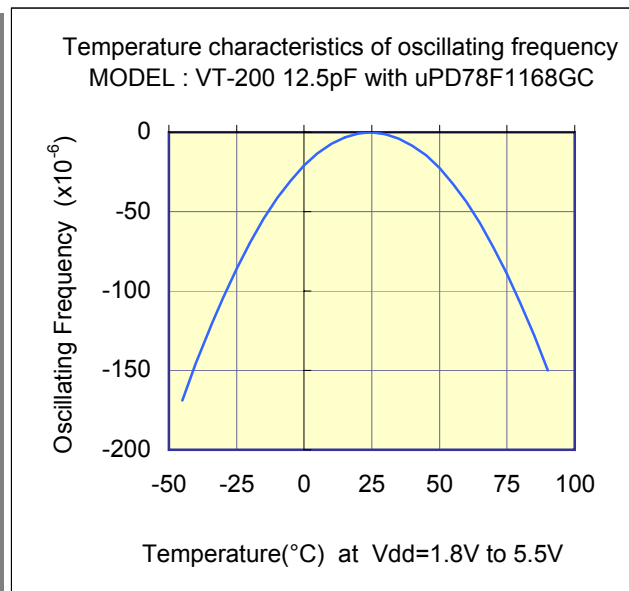
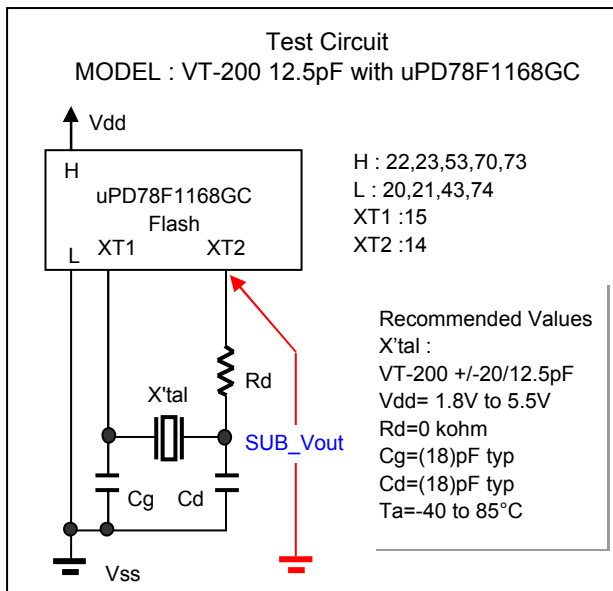
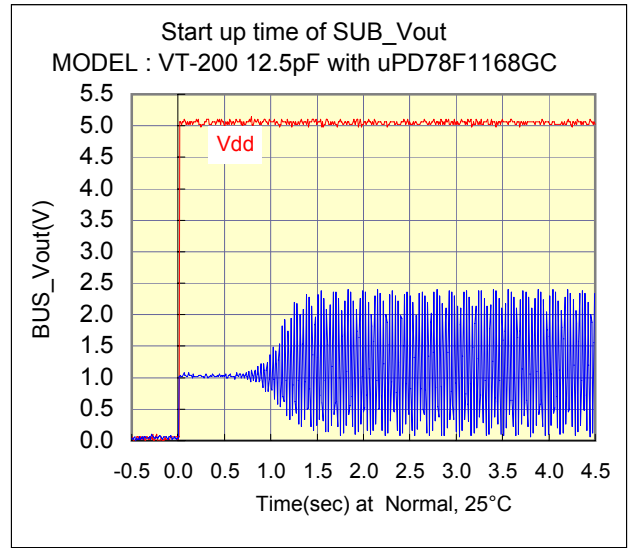
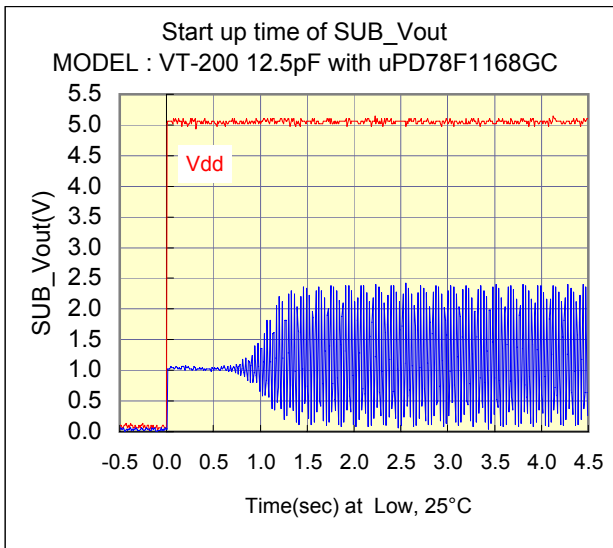
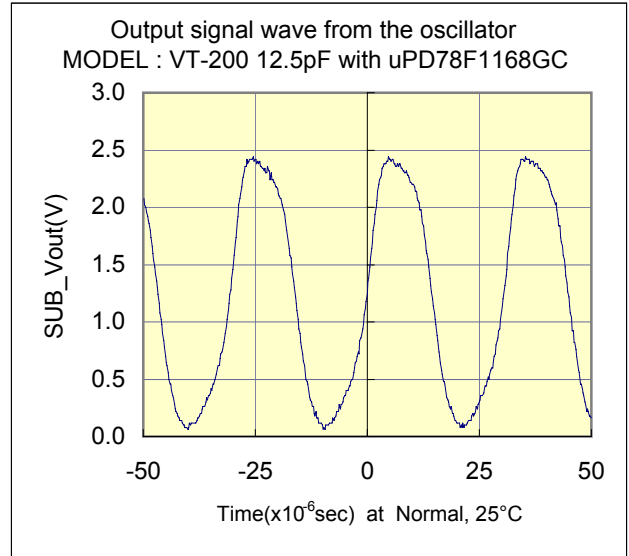
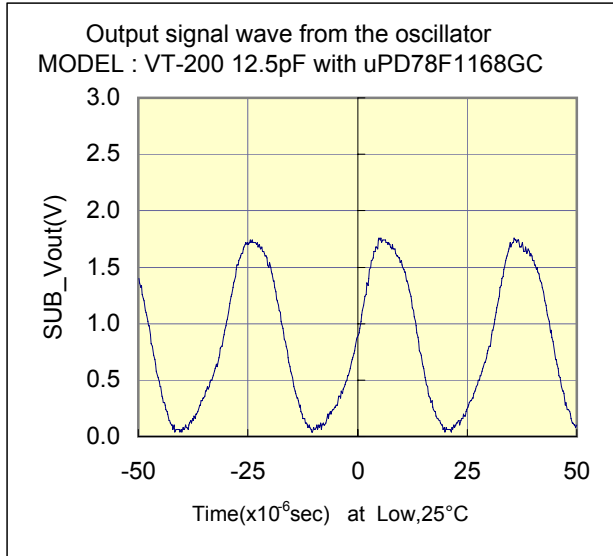
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Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch
 Measurement conditions : 5.0V



Test Data



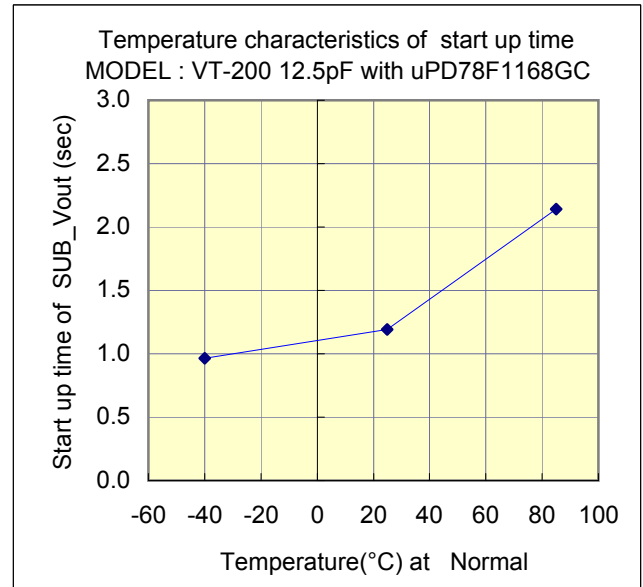
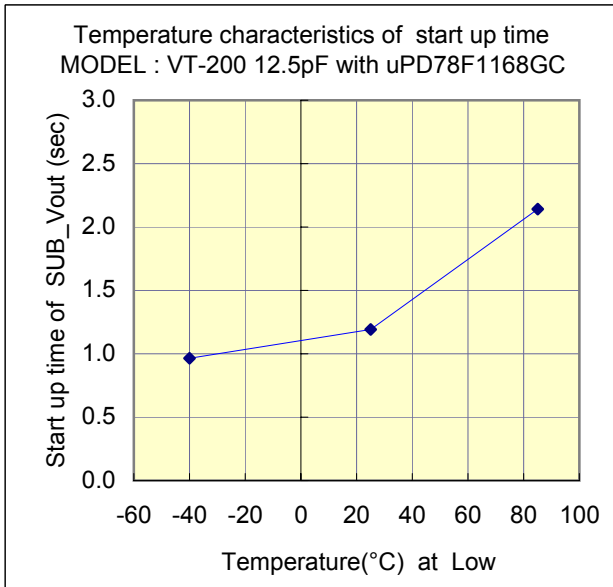
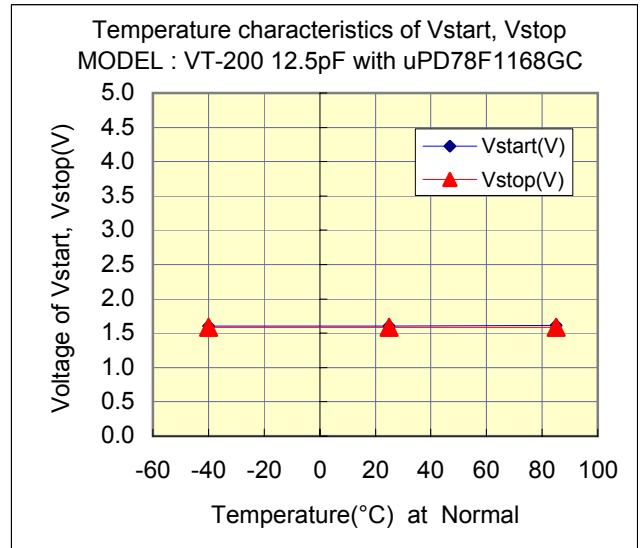
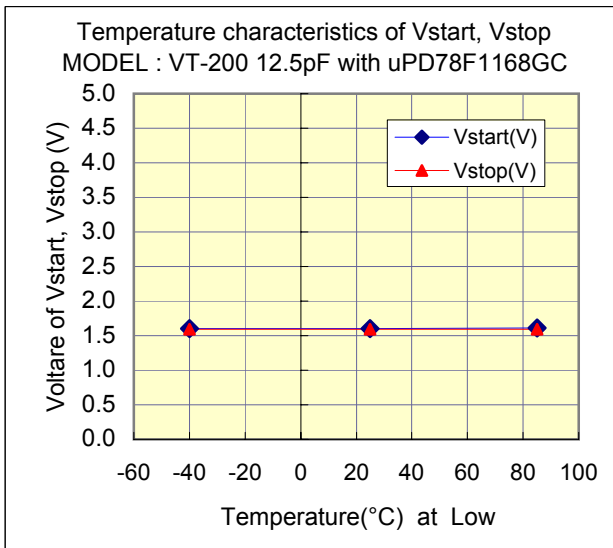
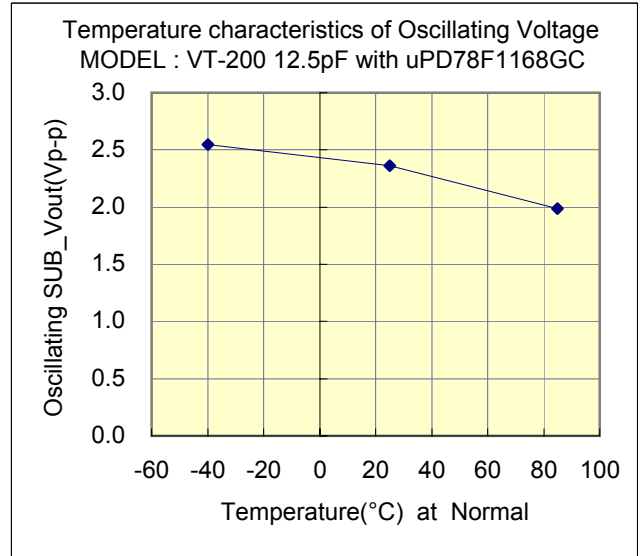
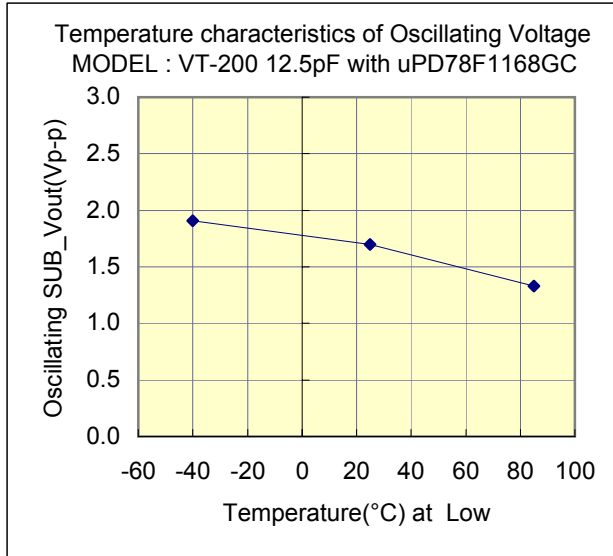
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



Test Data : Temperature characteristics



Evaluation of Subsystem Clock Oscillation Circuit

[μ PD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



Referential components layout(see Figure 1)

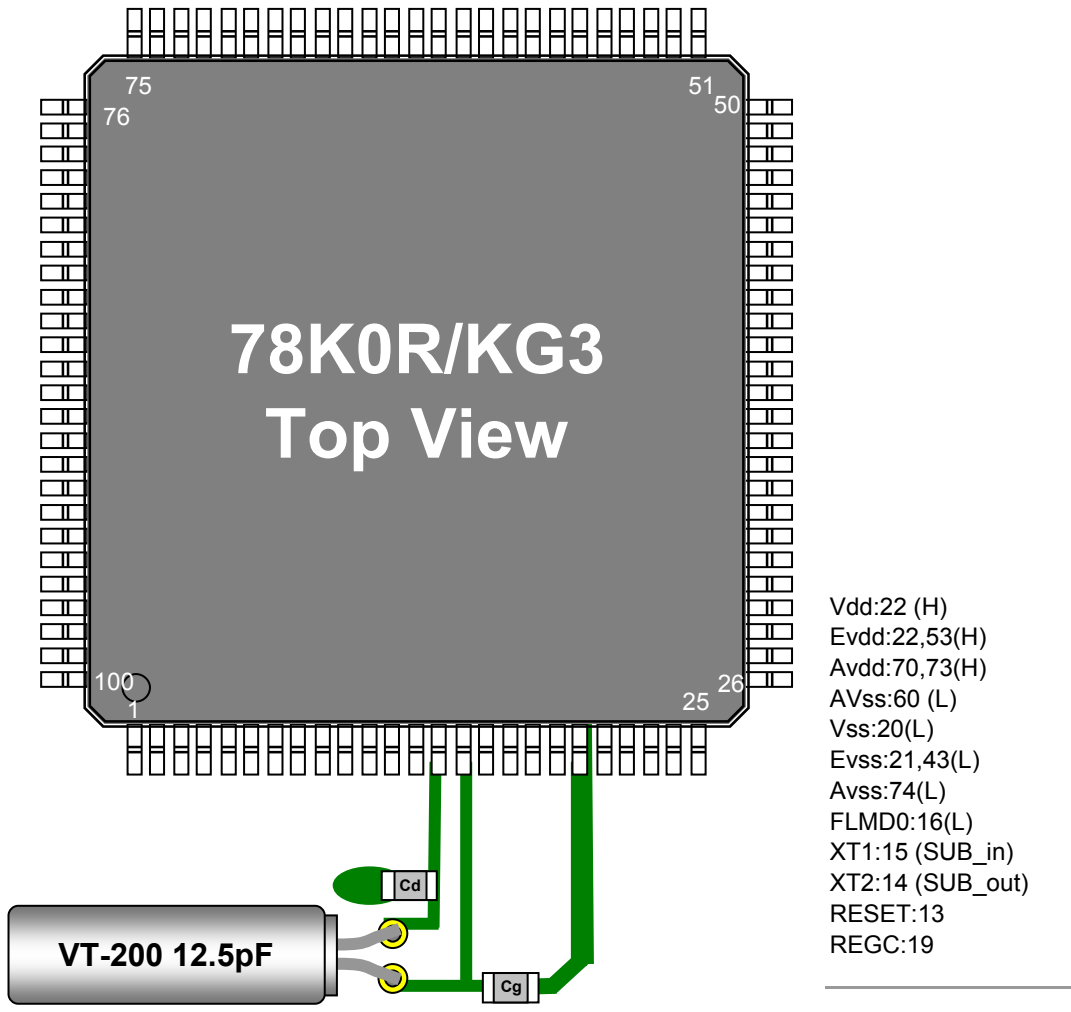


Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

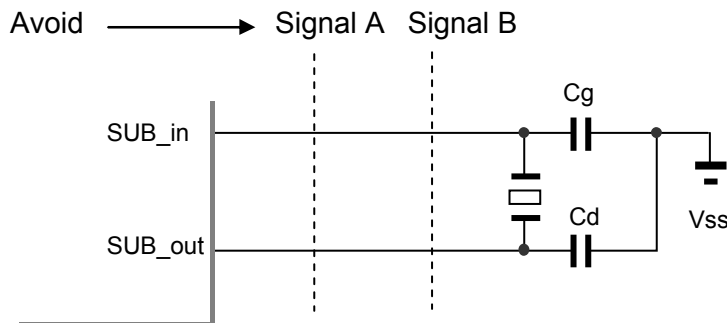


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors R_d in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



[Evaluation Sample : VT-200 12.5pF at 25°C]

| SAMPLE | No. | CL(pF) | Fo(Hz) | fr(Hz) | R1(kohm) | Co(pF) | C1(fF) | Q(k) |
|------------------|-----|----------|----------|----------|------------|----------|----------|--------|
| VT-200 12.5pF | 1 | 12.5 | 32768.11 | 32765.28 | 27.4 | 0.91 | 2.319 | 76.5 |
| | 2 | 12.5 | 32768.09 | 32765.24 | 26.9 | 0.89 | 2.333 | 77.4 |
| | 3 | 12.5 | 32767.83 | 32765.10 | 29.0 | 0.90 | 2.233 | 75.0 |

[IC Test Data : IC Sample Rd=0 kohm,Cg=18pF,Cd=18pF at 25°C]

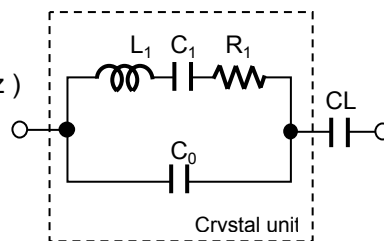
| Power mode | IC Sample | Fosc(Hz) | df / f(x10 ⁻⁶) | DL(x10 ⁻⁶ W) | -RL (kohm) | Vstart(V) | Ts(sec) |
|------------|-----------|------------|-----------------------------|-------------------------|---------------|-------------|---------|
| Normal | TYP | 32767.99 | 4.88 | 0.22 | 303 | 1.60 | 1.19 |
| | HH | 32767.97 | 4.27 | 0.24 | 273 | 1.60 | 1.33 |
| | HL | 32768.00 | 5.07 | 0.22 | 333 | 1.59 | 1.12 |
| | LH | 32767.97 | 4.12 | 0.24 | 273 | 1.67 | 1.32 |
| | LL | 32767.99 | 4.73 | 0.22 | 333 | 1.59 | 1.10 |

[IC Test Data : IC Sample Rd=0 kohm,Cg=18pF,Cd=18pF at 25°C]

| Power mode | IC Sample | Fosc(Hz) | df / f(x10 ⁻⁶) | DL(x10 ⁻⁶ W) | -RL (kohm) | Vstart(V) | Ts(sec) |
|------------|-----------|------------|-----------------------------|-------------------------|---------------|-------------|---------|
| Low | TYP | 32767.90 | 2.14 | 0.13 | 183 | 1.60 | 1.19 |
| | HH | 32767.89 | 1.68 | 0.13 | 163 | 1.60 | 1.33 |
| | HL | 32767.92 | 2.75 | 0.14 | 213 | 1.59 | 1.12 |
| | LH | 32767.88 | 1.53 | 0.12 | 163 | 1.67 | 1.32 |
| | LL | 32767.92 | 2.75 | 0.14 | 213 | 1.59 | 1.10 |

Remark (see figure 3)

$$Fo = fr \times \{ C1 / (2 \times (Co + CL)) + 1 \} \text{ (Hz)}$$



Fo : Load resonance frequency
 fr : Resonance frequency
 R1 : Motional resistance
 C1 : Motional capacitance
 Co : Shunt capacitance
 CL : Load Capacitance

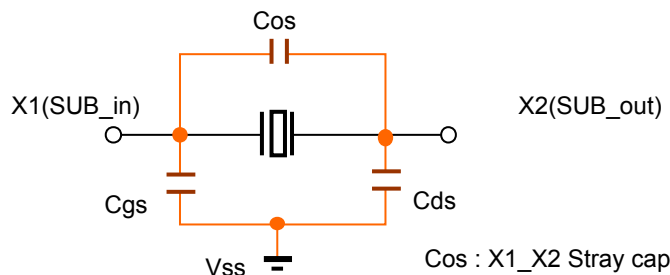
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \text{ (pF)}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
 Cgs : X1_Vss Stray capacitance
 Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : Vdd=(1.6V) to (6.0V) at 25°C

Referential Data : Voltage characteristics

