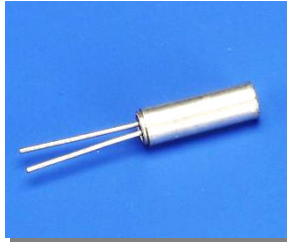


Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : 3.3V

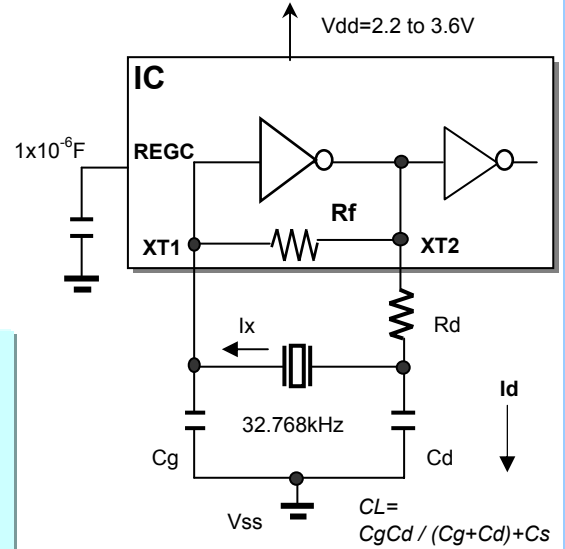
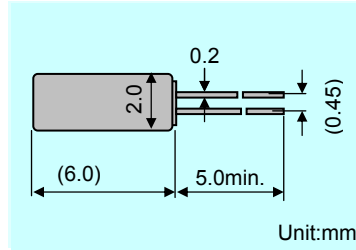


Model :VT-200
 Frequency :Fo=32.768kHz
 Frequency tolerance :dF/Fo= +/-20x10⁻⁶
 Load capacitance :CL=12.5pF
 Equivalent series resistance :R1=50kohm max
 Max. drive level :DL=1x10⁻⁶W max
 Level of drive :DL=0.1x10⁻⁶W typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) Ix : current through crystal

MODEL:VT-200 12.5pF with uPD70F3738GC at 25°C

Key specifications	Low(*1)	Normal(*2)	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	18	18	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	18	18	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Low(*1)	Normal(*2)	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	4.7	6.1	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.15	0.24	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	193	303	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	4	6	Judgemental standard of oscillation stability
consumption current : Id (nA)	1,201	1,615	Cd charge current, Id = ωCd*Vd
Voltage of oscillation start : Vstart (V)	1.22	1.22	
Voltage of oscillation stop : Vstop (V)	1.05	1.05	
Oscillation start up time : Ts (sec)	1.20	1.20	Time to reach 90% of output level

Temperature characteristics of circuit	Low(*1)	Normal(*2)	Remarks
at -40°C Variation : df / T (x10 ⁻⁶)	-139	-139	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C Variation : df / T (x10 ⁻⁶)	-126	-126	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

*1; low consumption current mode
 *2; normal current mode

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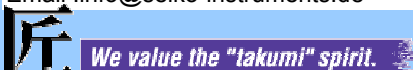
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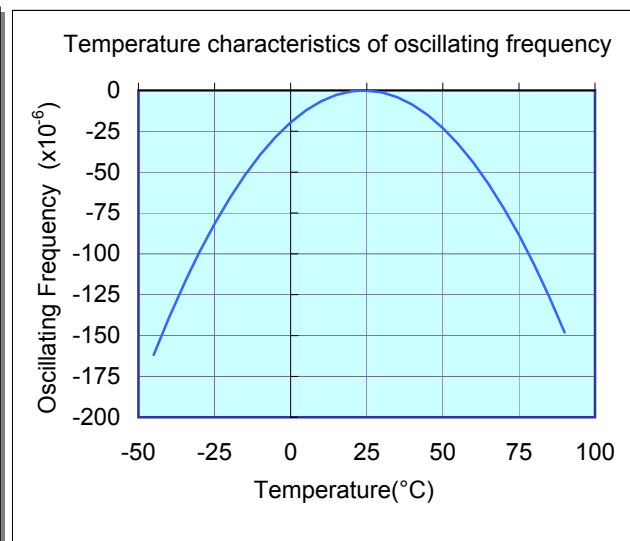
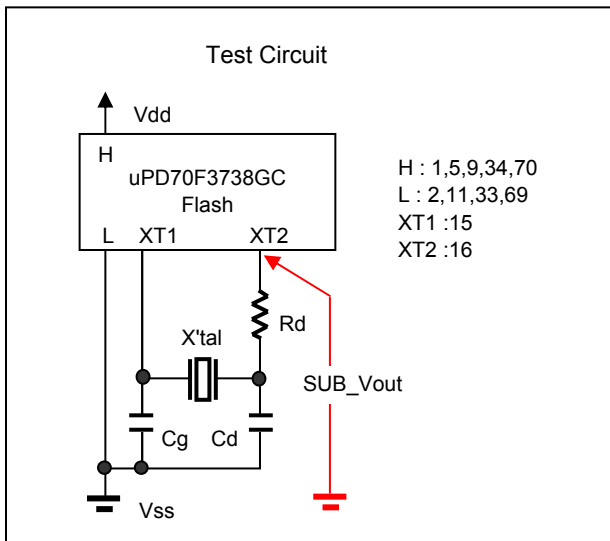
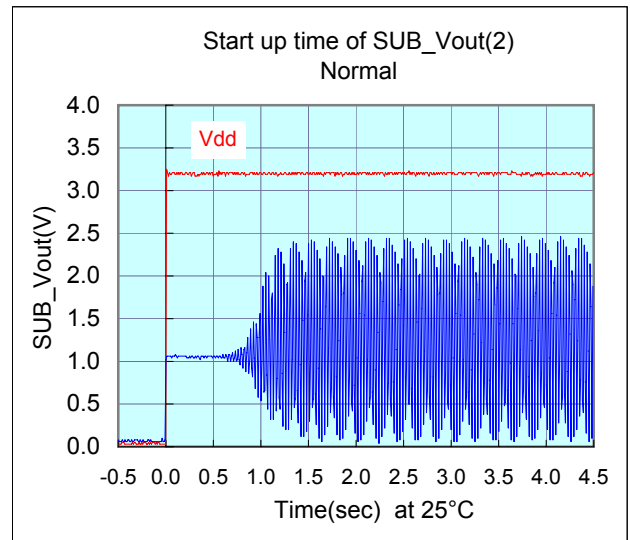
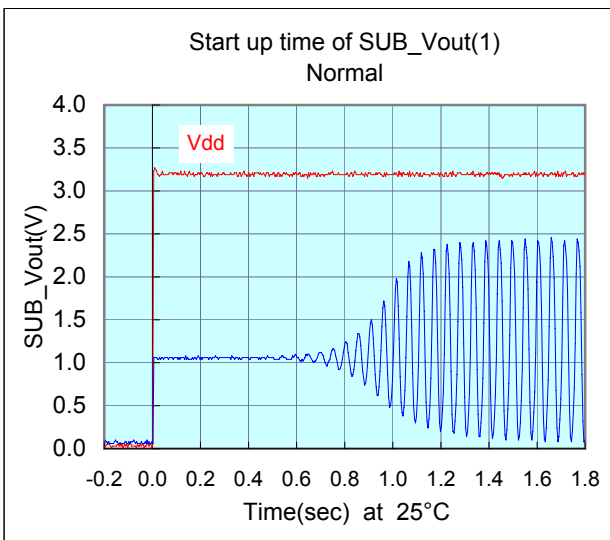
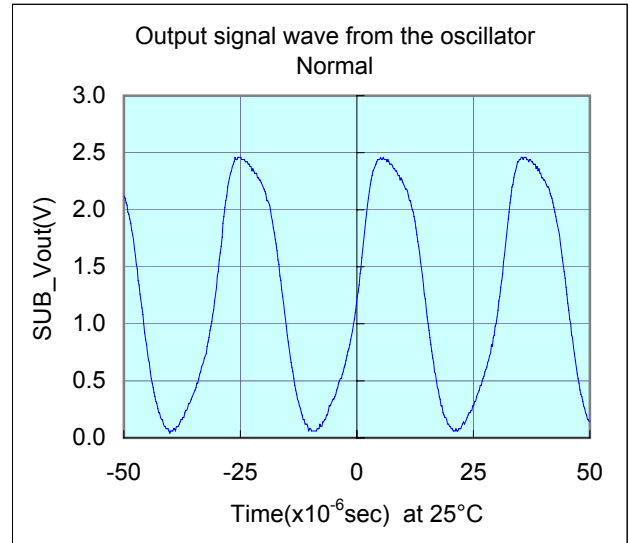
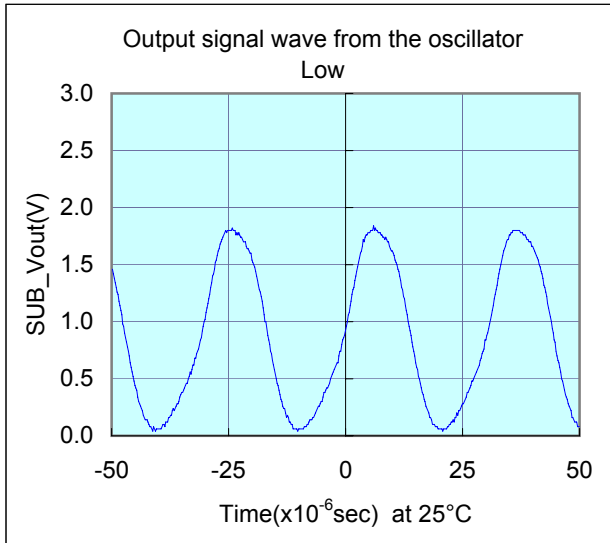
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

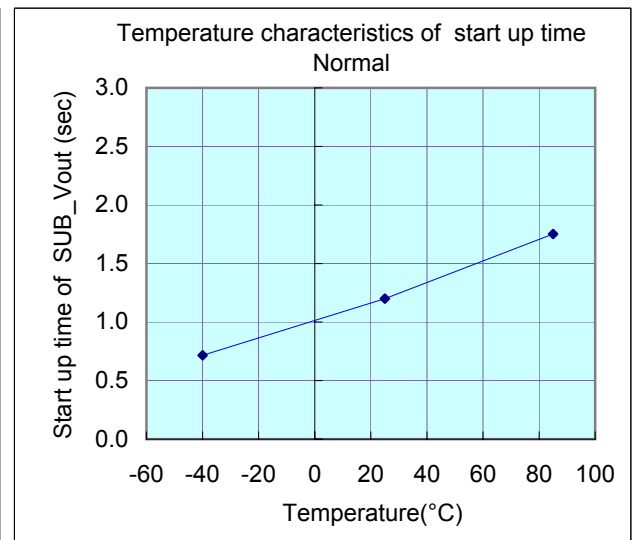
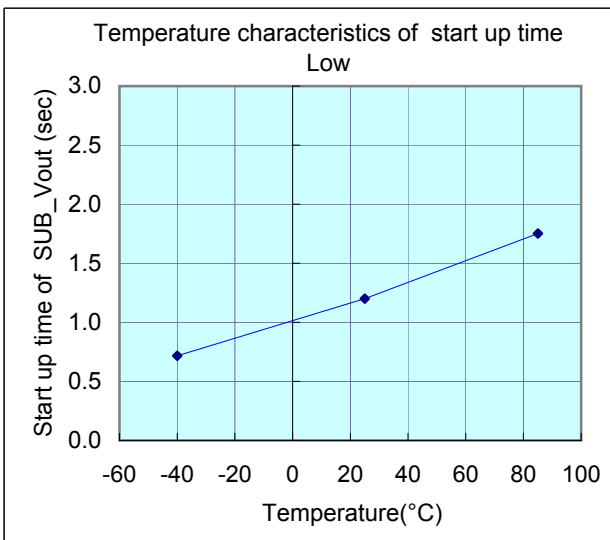
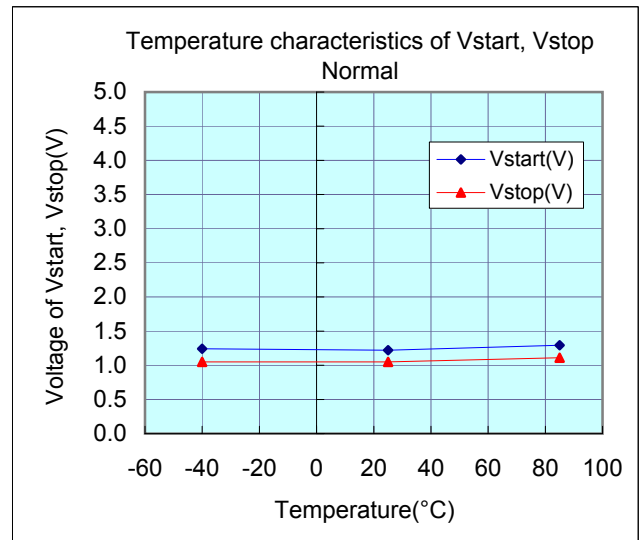
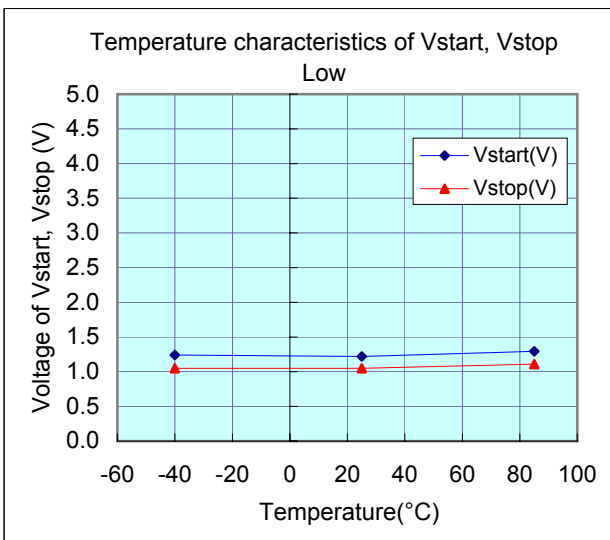
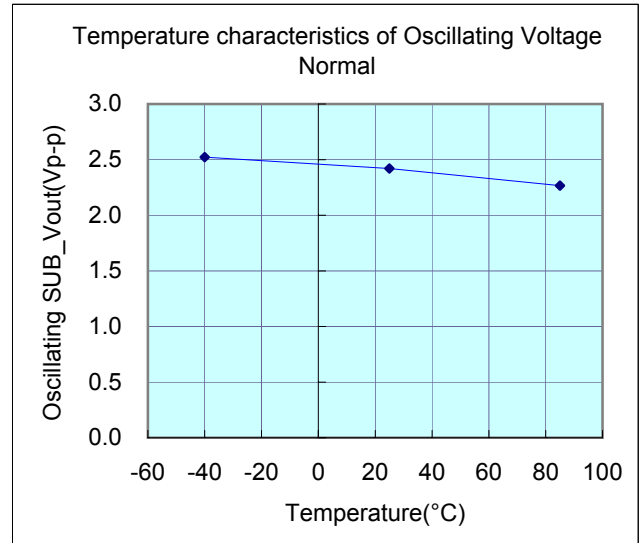
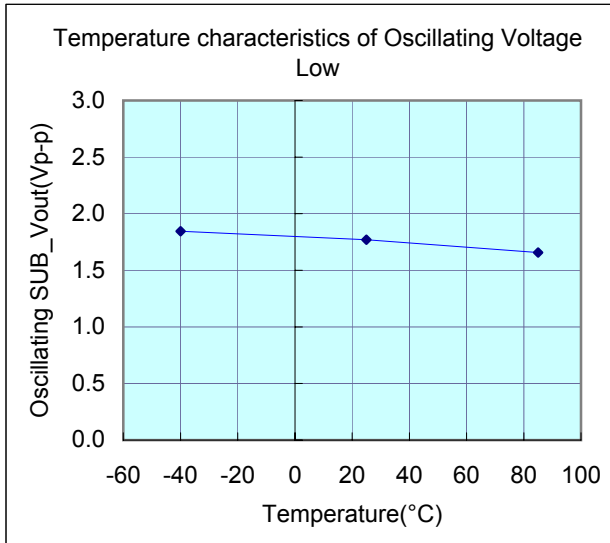
Measurement conditions : 3.3V



Test Data



Test Data : Temperature characteristics



Referential components layout(see Figure 1)

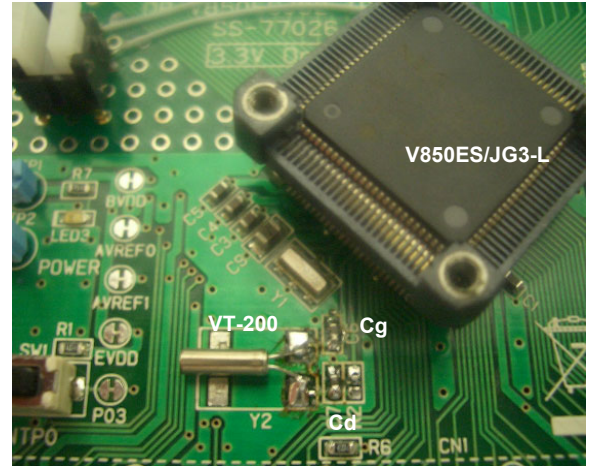
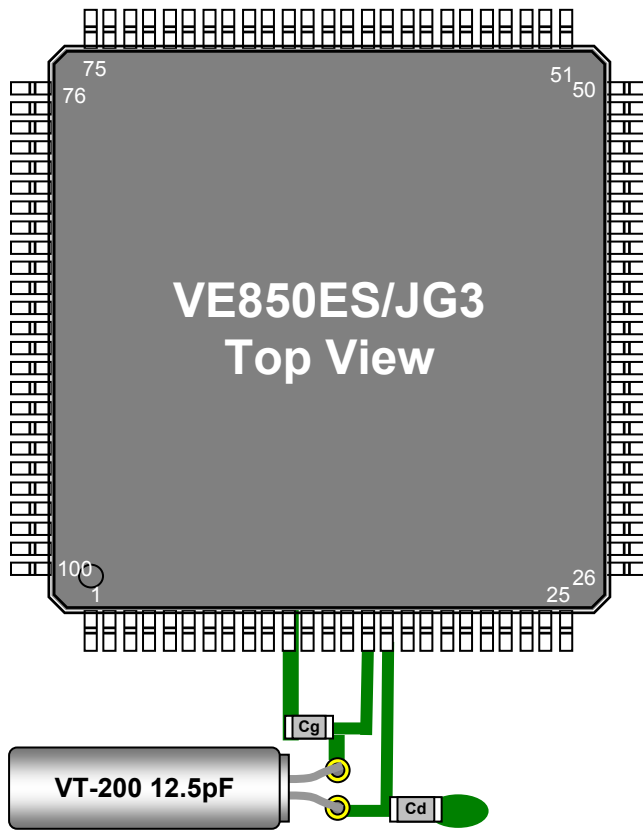


Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

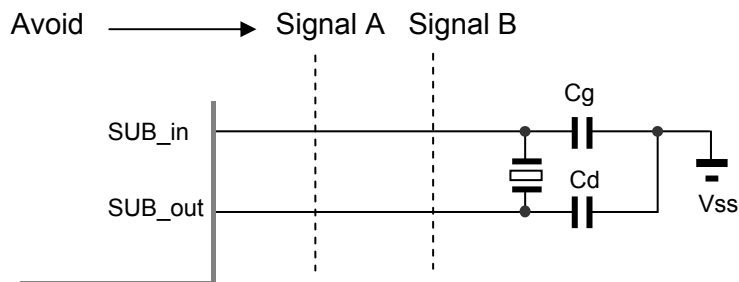


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : 3.3V



[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 12.5pF	1	12.5	32768.30	32765.60	27.8	0.89	2.207	79.2
	2	12.5	32767.65	32764.49	27.8	0.89	2.583	67.7
	3	12.5	32767.83	32765.10	29.0	0.90	2.233	75.0

[IC Test Data : IC Sample Rd=0 kohm,Cg=18pF,Cd=18pF at 25°C]

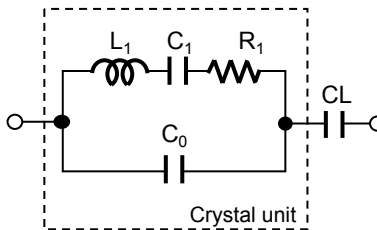
mode	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm	Id (nA)	Vstart(V)	Ts(sec)
Normal	TYP	32768.03	6.10	0.24	303	1,615	1.22	1.20
	HH	32768.03	5.95	0.26	273	1,618	1.32	1.50
	HL	32768.03	6.10	0.24	303	1,635	1.20	1.16
	LH	32768.02	5.80	0.25	273	1,642	1.32	1.55
	LL	32768.04	6.41	0.23	333	1,629	1.18	1.12

[IC Test Data : IC Sample Rd=0 kohm,Cg=18pF,Cd=18pF at 25°C]

mode	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm	Id (nA)	Vstart(V)	Ts(sec)
Low	TYP	32767.99	4.73	0.15	193	1,201	1.22	1.20
	HH	32767.99	4.27	0.15	163	1,188	1.32	1.50
	HL	32767.98	4.58	0.15	193	1,204	1.20	1.16
	LH	32767.97	4.27	0.14	163	1,195	1.32	1.55
	LL	32767.99	4.88	0.15	213	1,219	1.18	1.12

Remark (see figure 3)

$$F_o = f_r \times \{ C_1 / (2 \times (C_o + C_L)) + 1 \} \text{ (Hz)}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

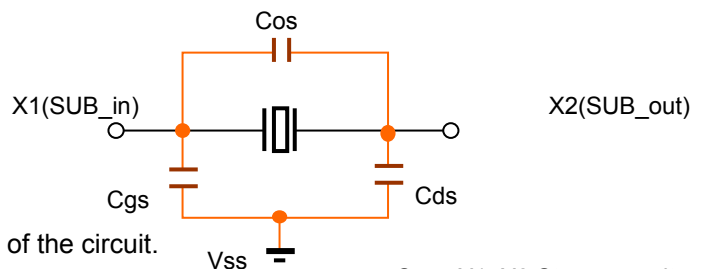
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



- Cos : X1_X2 Stray capacitance
- Cgs : X1_Vss Stray capacitance
- Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : Vdd=(1.8V) to 3.6V at 25°C



Referential Data : Voltage characteristics

